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## Tittle:

Image Capture and Processing of an FPGA Based Real time Driver Drowsiness Detection System.

## Abstract:

This research focuses on the image capturing and image processing of the Driver Drowsiness Detection System. The image capturing process required several process steps. The proposed architecture uses a 5 Mega pixels Terasic CMOS camera to capture the RAW image from the driver’s face. The RAW image captured will be converted into an RGB format. The image processing is then separated into two sections which are the image segmentation and the image compression. The task for the image segmentation process consists of RGB to grayscale and binary conversion using thresholding method. The image is localized by tracking the edge of the binary image. The Grey scaled image referring to the localized coordinate of each eye is then passed to perform Discrete Cosine Transform (DCT) compression. An HDL based test-bench will be created for each sub-blocks for verification purpose in Modelsim in Mentor Graphic Environment before implementation on the Cyclone IV FPGA can be performed. After all verification has been done, two 1-bit 10x10 matrix will be passed into the recognition block to drowsiness detection. The Driver Drowsiness Detection System is designed to reduce the accident rate. Thus, the accuracy of the output is the demand of this system. The image taken in this research will be directly captured from the driver face but not from the CASIA database as in the past researcher by using the D5M camera to capture the image of the iris from the CASIA database. The expected accuracy of this design would be at 90%. With the DCT compression used in this design compared to the past researcher using Harr Wavelet, speed will be improved by 5%. This proposed research gives advantages on the road safety, this system can work as a built-in system for each vehicle on the road. This system also can be applied on any other application that wants to avoid the user to fall asleep.

## Objective:

1. To investigate the architecture of the image capturing and image processing of the drowsiness detection system. The image compression includes the image segmentation and DCT image compression from the past review.
2. To model, design and simulate the drowsiness detection system which involves image capturing and image processing using Verilog HDL in Modelsim environment.
3. To analyze, integrate and implement the design Verilog Codes of the image capturing and image processing of the drowsiness detection system using FPGA for functional verification.

## Introduction:

In today’s world, most of the people are driving vehicles. For a driver that drive for hours, they will easily falls asleep or loose concerntration while they are driving. This may cause serious accident when the driver fall asleep. Thus, the drowsiness detection system has been proposed to potentially avoid the stated problem.

The capabilities of this system is to detect whether the driver is sleepy or alert while driving. There are many ways to detect the drowsiness of the driver, which is either to detect the motion of the head, the eye closing interval and the yawning action. Current research, reduces the drowsiness detection complexity of the design by only detecting the eye closing interval (Kuo and Hsu 2010). The reason not to detect the yawning of the mouth is because the driver might be talking but not yawning when the mouth is opened. Hence, the result obtained will be inaccurate.

From almost all the past research, there are only a few that are implementing the drowsiness detection system using hardware. They usually used software based methods to directly program to the microprocessor which do not require comprehension of the low level operations. This work implements the drowsiness detection system using hardware based methods.

The method of capturing of the driver’s face will be based on the design by Yap (2015). In which Image capture of the iris is performed while in this research the entire face is captured. There are some modification made in order to achieve this objective. The method of localization in this design is used thresholding. Hence, this method can be applied to localize the eye of the driver. The localized image will be compressed by using the Discrete Cosine Transform (DCT) method.

There are several techniques to perform image capturing and compression. Some of it has been listed down in table 1 for the reference. For image capturing, in Yap and Chuah (2009) work has used the D5M CMOS camera to capture the image and localize the image by using thresholding method to perform Iris Recognition System (IRS). This system also perform image normalization and compression. The compression technique used in this design is by Haar Wavelet. There are also other technique of doing image compression like in the design Kassem (2009) using DCT compression with Lee algorithm and the design of Mathur (2012) using DFT through Fast Fourier Transform Technique to perform image compression. In Flores (2008) and Acasandrei (2012) architecture, they both used Viola Jones algorithm to track the location of the human face. Alternatively, the Architecture of Wang (2005) is using Nios II soft core embedded processor to perform Drowsiness Tracking System.

In summary, this work uses the D5M CMOS camera to capture the image of the driver. The face was localized using thresholding method. The captured image is then been processed and compressed using DCT compression.

Table 1 Past Literatures on the Image Processing for Drowsiness Detection System.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| No. | Researcher (Year) | Architecture/System | Method applied | Results |
| 1 | Kassem etal. (2009) | Image Compression on FPGA using DCT | This paper presents a method to implement the DCT compression technique using Lee algorithm | The Maximum percentage error of 8% on the pixel range [0,256]. |
| 2 | Wang  etal.  (2005) | Real-Time Driver Drowsiness Tracking System | This design adopts the Altera Nios II soft core embedded processor and combines image processing and mode identification functions | Reduced complexity using NIOS II with correct Judgment rate of 62.5% and 80ms response time |
| 3 | Acasandrei  and  Barriga  (2012) | FPGA Implementation of an Embedded Face Detection System based on LEON3 | Using Viola Jones algorithm with integral image to perform face detection. | The estimate static power consumption for the LEON3 core is 603mW |
| 4 | Mathur etal. (2012) | Image Compression Using Dft through Fast Fourier Transform  Technique | Image compression method based on Fast Fourier Transformation. | The compression ratio is very good but the image quality degrades as the  compression ratio is increased |
| 5 | Flores etal.  (2008) | Real-Time Drowsiness Detection System for an Intelligent Vehicle | Advanced Driver Assistance System for automatic driver’s drowsiness detection based on visual information and Artificial Intelligence. | It has a minimum of 91.61% of correct detection rate. |
| 6 | Yap and  Chuah (2015) | Iris Normalization and Iris Feature Extraction implemented using FPGA | Compression of the iris region into a 10x10 array is based on Discrete Haar Wavelet Transformation (HWT). | The power consumption for the compression module is 123.36 mW |

## Problem Statement:

The proposed work addresses the problems faced by the first conventional technique by Yap (2015) and Chuah (2015). In this research, the images will be captured directly from the human face but not from CASIA database. Also the design will be improved by replacing Discrete Haar Wavelet Transformation (HWT) with Discrete Cosine Transform (DCT) to enhance speed.

The second conventional technique (Kassem 2009) is an example of implementing the DCT image compression. In this technique, it consists of compression and decompression. This research will implement the hardware compression represented by the DCT equation. The equation of DCT can be referred in Kassem’s (2009) work.

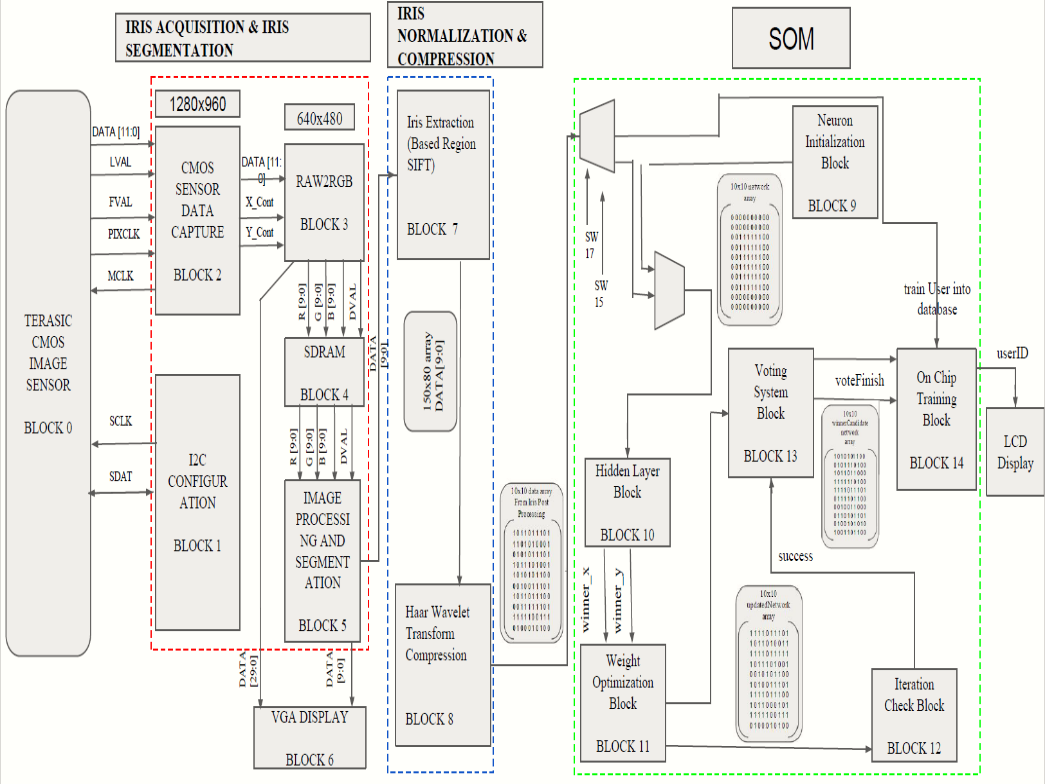


Figure 1 Conventional Block for Image Capture and compress. Yap and Chuah (2009).

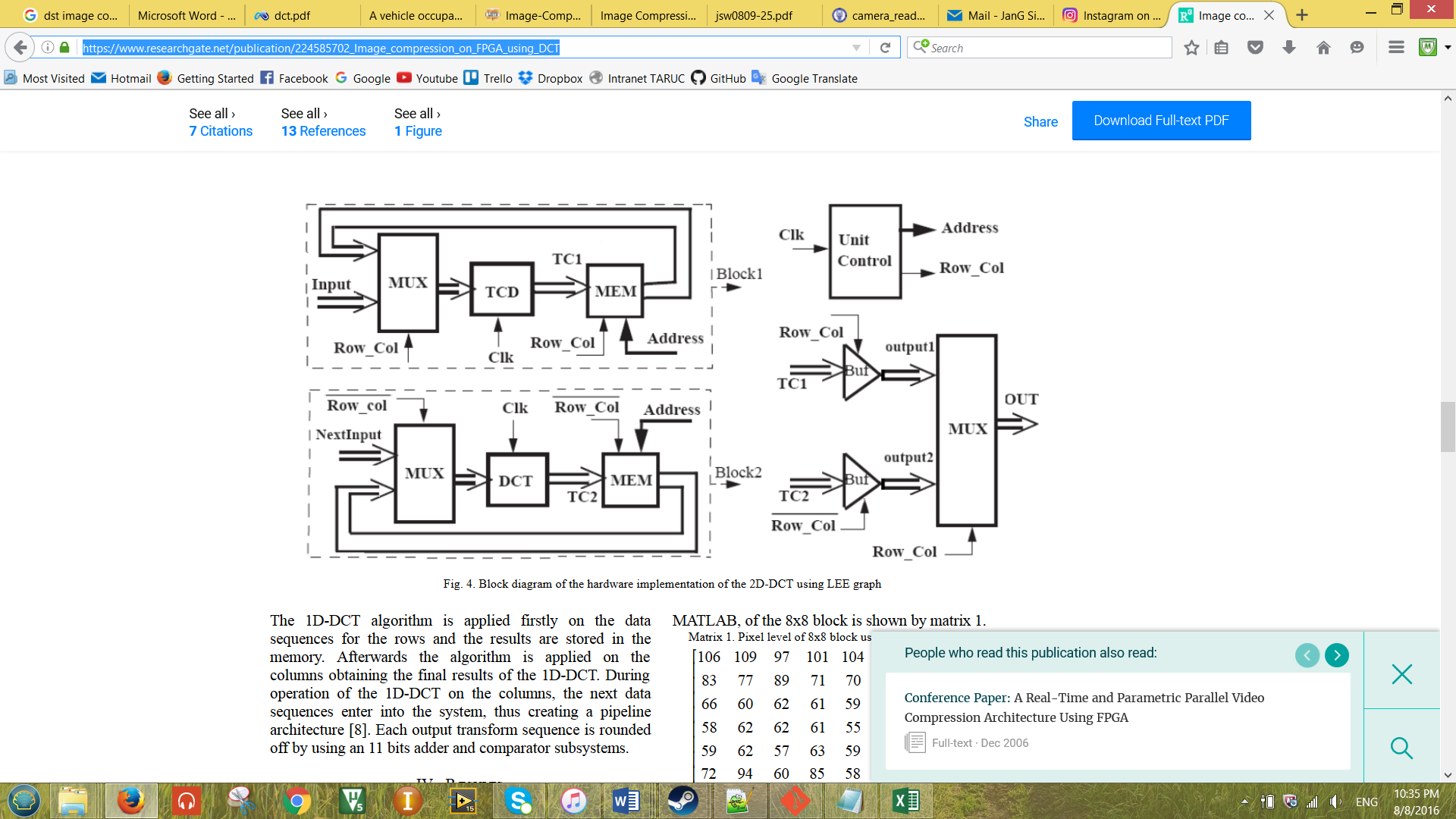


Figure 2 Conventional Block for DCT Image Compression.(Kassem 2009)

## Proposed Block:

The proposed Drowsiness Detection Block is as shown in Figure 3 and it contains two main sections. The first section is the Image Capturing and Image Processing. This section will capture the image of the driver’s face and process the image by segmenting the two eyes of the driver and compresses the image for the second section. The second section is the image recognition portion which determines whether the driver’s eye closes or not. This work focuses on the Image Capture and processing section of the Drowsiness Detetion System as shown in Figure 4.

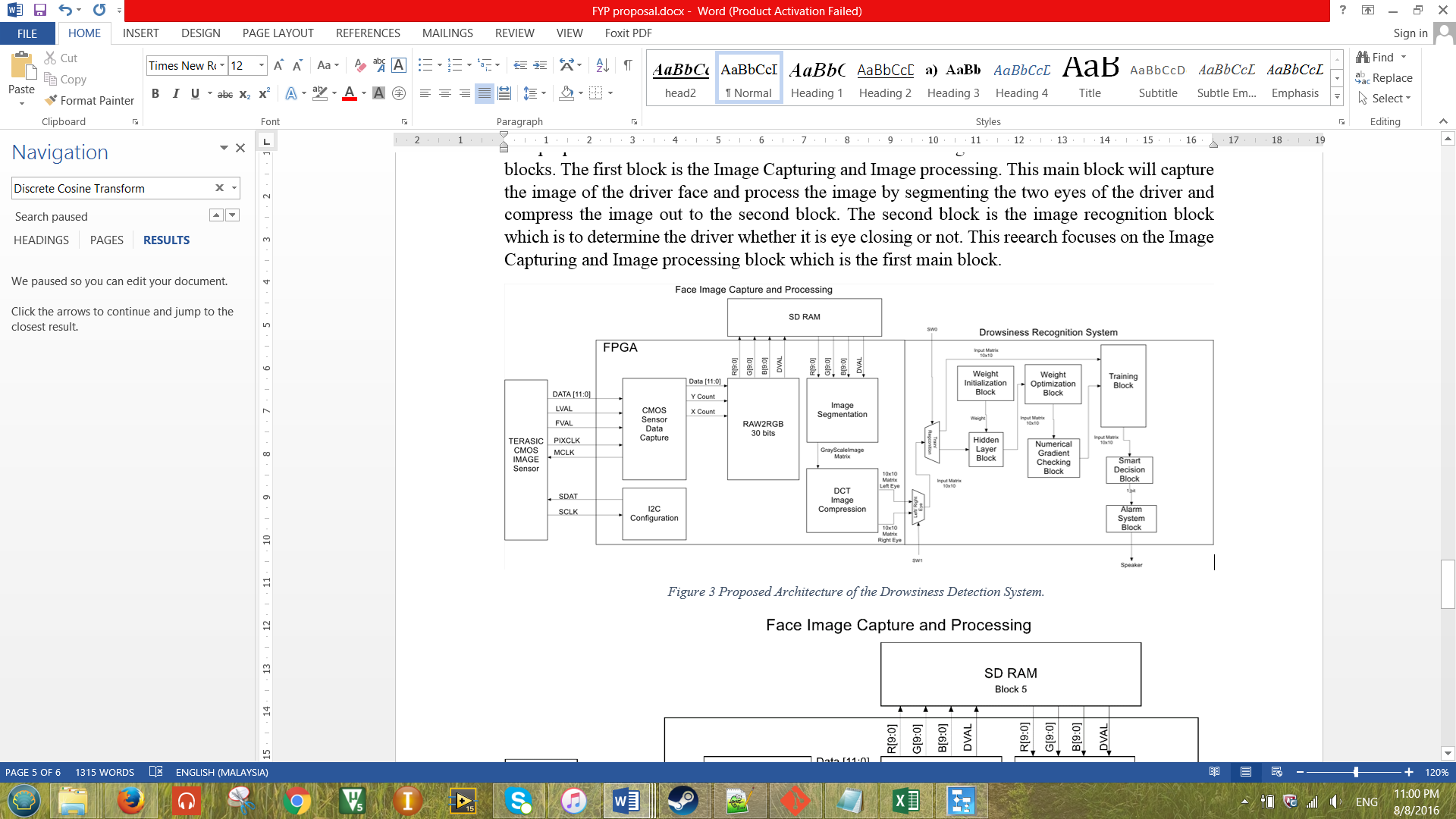


Figure 3 Proposed Architecture of the Drowsiness Detection System.

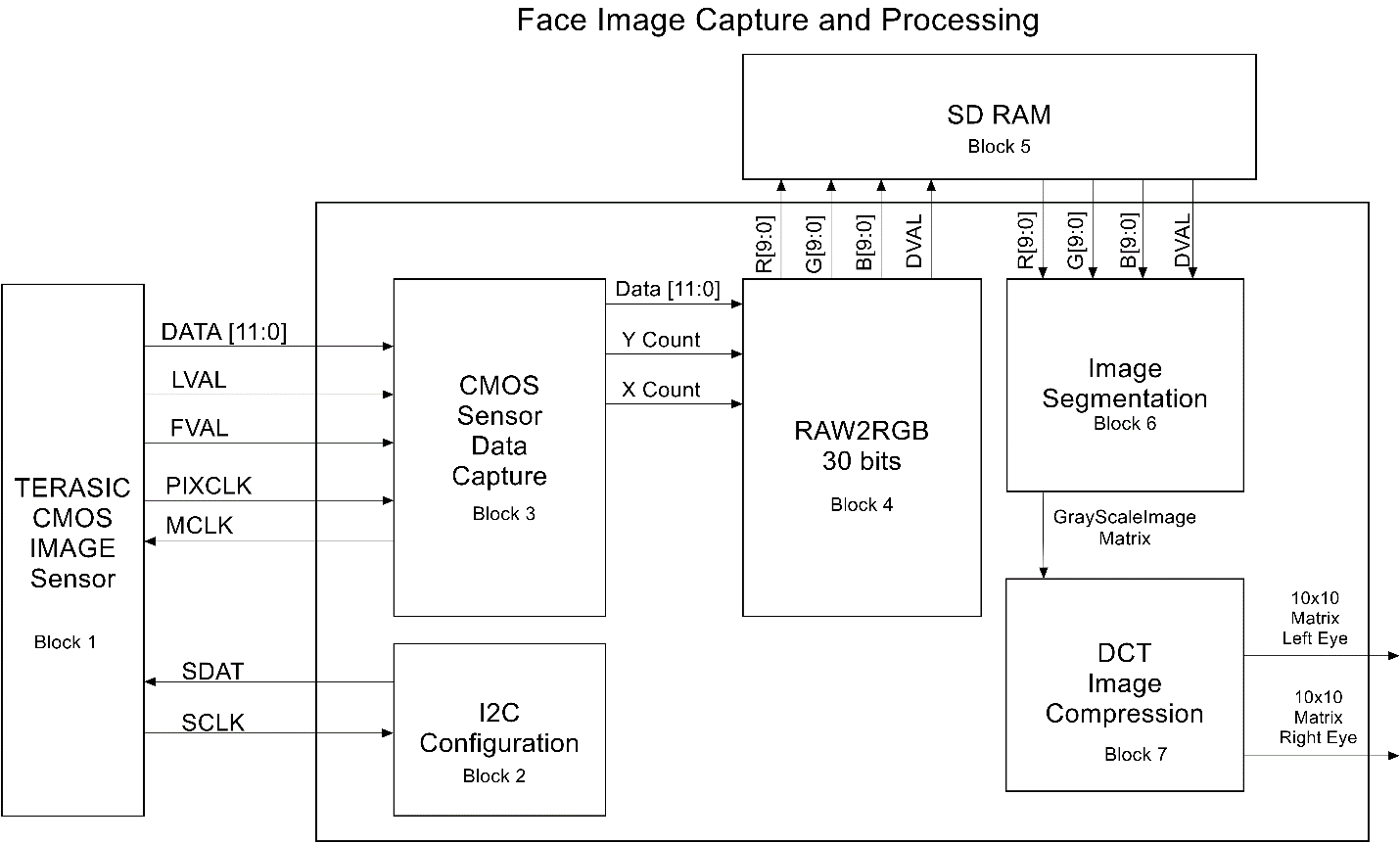


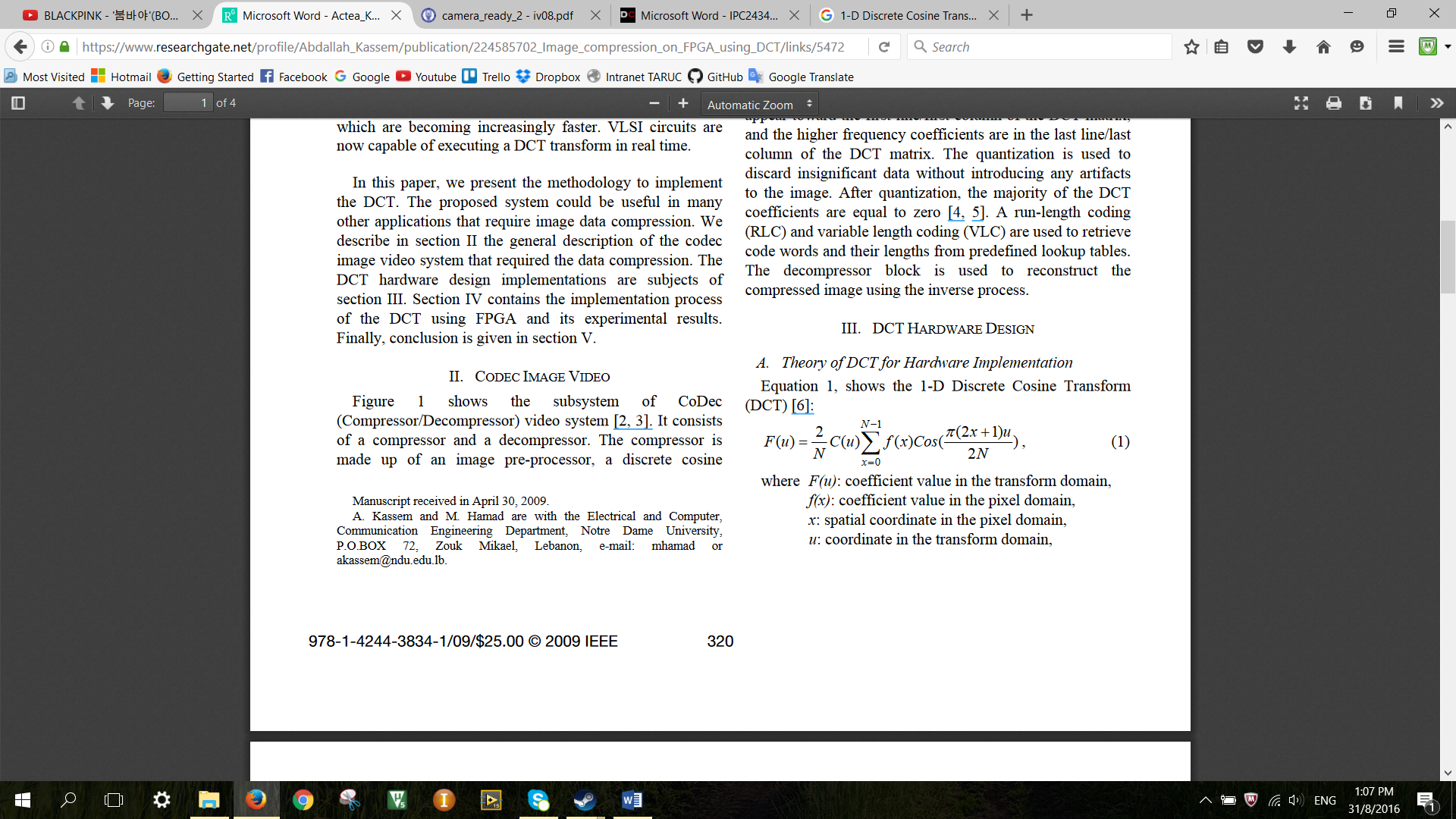
Figure 4 Proposed Architecture for the Image Capture and Processing of the Drowsiness Detection System.

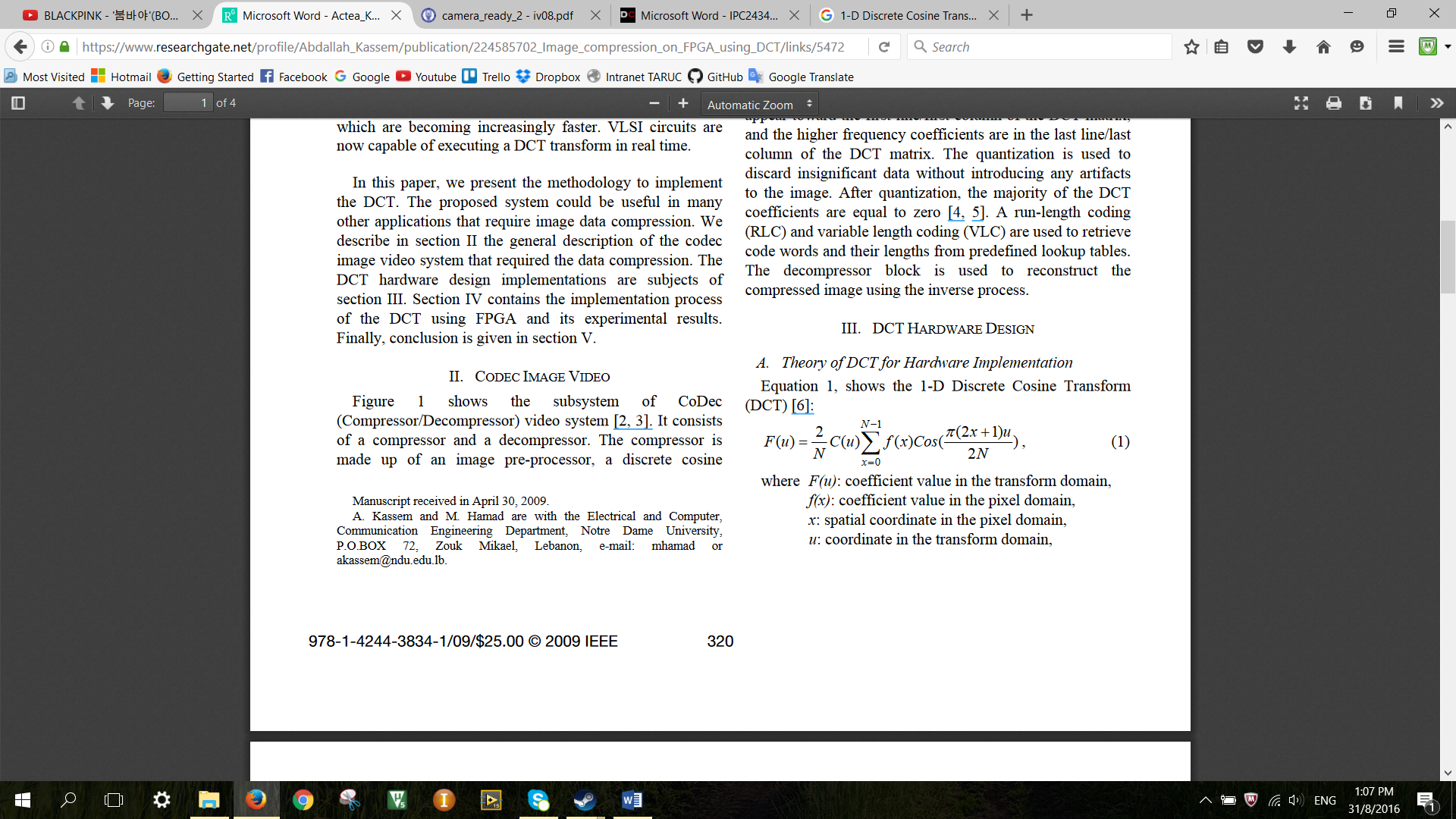
Firstly, the CMOS Sensor Data Capture (Block 1) will send appropriate signals to the second block when it received command by the I2C (Block 2). The CMOS Sensor Data Capture (Block 3) receives signal to begin image data capture. The captured RAW data is then converted to RGB format by the RAW2RGB (Block 4). The image with RGB format is then been stored into the external SDRAM (Block 5) in the form of a 30 bits per element 640x480 matrix.

For the second part of this main block would be the processing part. The processing part consists of two parts which is the Segmentation block (Block 6) and the DCT Image Compression block (Block 7). The segmentation block will receives the matrix that has been stored in the SDRAM previously and converts it to grayscale and binary format by using the thresholding method. The 1-bit per element 10x10 matrix obtained from the compression block will be fed into the drowsiness recognition system for the driver drowsiness detection purposes.

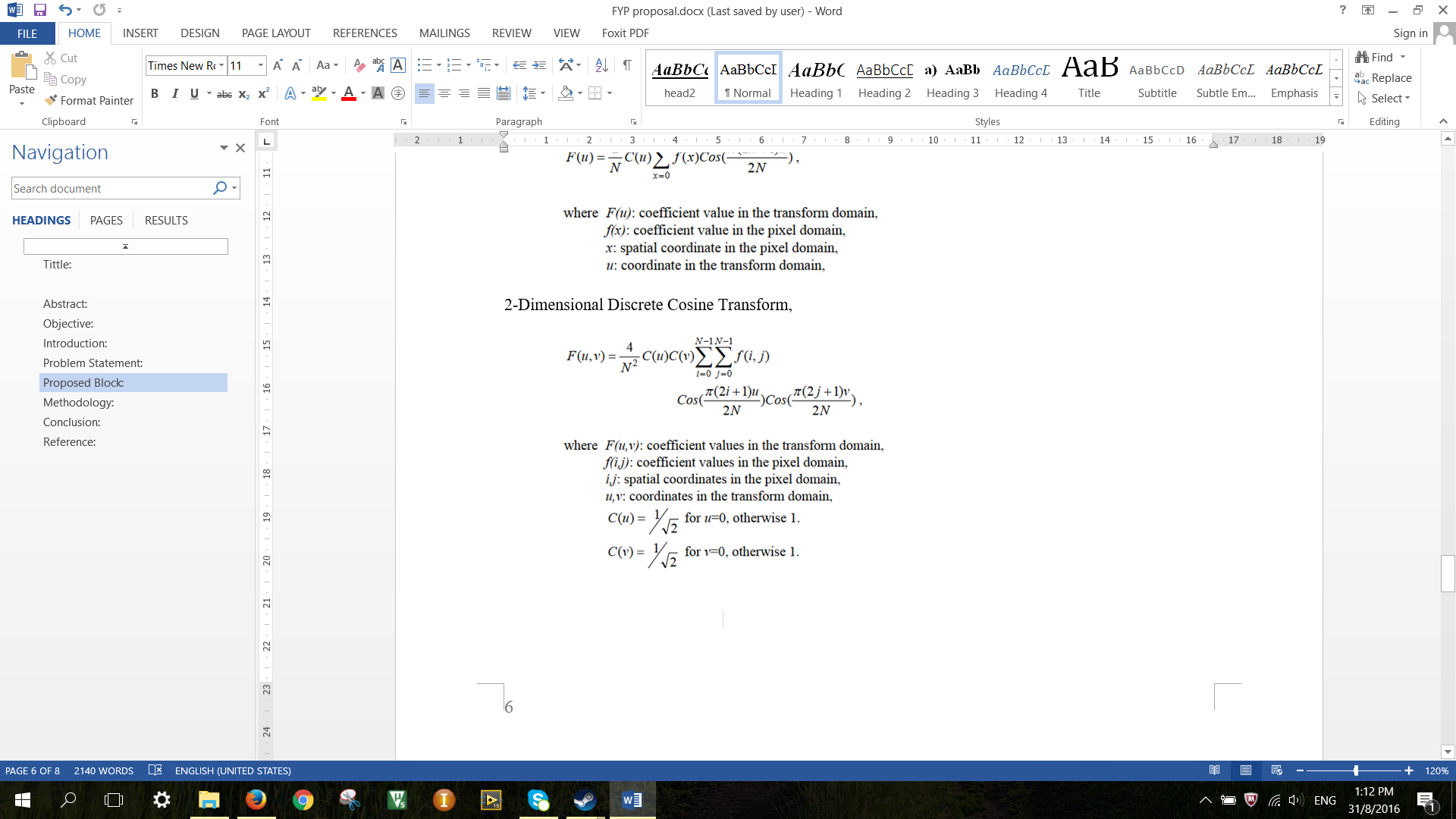
The contribution of this work will be at the image compression block. From the previous architecture from Yap and Chuah (2015), the design perform compression using Haar Wavelet. While in this work is using DCT compression. The equations of the DCT compression is as shown below.

1-Dimensional Discrete Cosine Transform,





2-Dimensional Discrete Cosine Transform,



## Methodology:

Figure 5 shows the design flow chart of the image capture and compression of the Drowsiness Detection System. The description for each block will be discussed in this section.

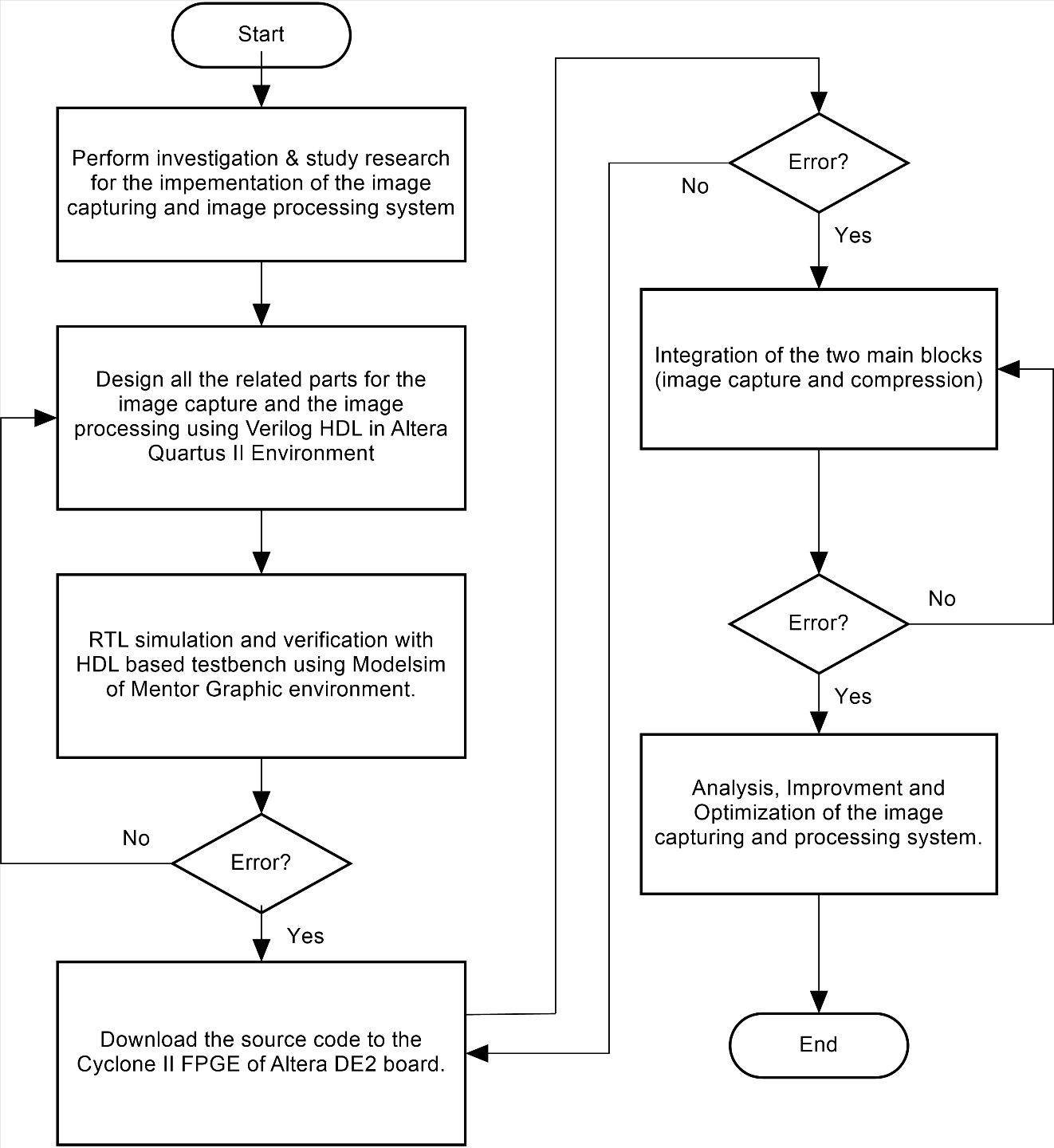


Figure 5 Design Flow Chart for the Drowsiness Detection System.

The first step of the design is to investigate through literature review regarding all sub-blocks related to the drowsiness detection system. After all sub-blocks has been investigated, these block will be modelled & designed by using Verilog HDL in Altera Quartus II. Each sub-block will be simulated by using Verilog HDL based testbench in Modelsim of Mentor Graphics environment. The result can be obtain from the waveform or console output produced by Modelsim. If there were any errors in the design, modification has to be made from the design source code. Eventually, the result also has to be verified with the hardware by downloading the program to the Cyclone II FPGA of Altera DE2 board.

If all the process mentioned above doesn’t incur any error, the hardware is now ready to be integrated with the recognition block. Error might occur during the integration process, so if there were any error during this stage, some modification has to be made on one of the designs.

## Conclusion:

The Drowsiness Detection system is divided into two parts which are the ‘Image Capture and Processing’ as well as the ‘Image Recognition and Tracking’. This research focusses on the implementation of compression by using DCT. The image will be captured by using the Terasaic CMOS camera and segmented using the thresholding method. This research will be designed by using Quatus II and verified by ModelSim using HDL based testbench. The expected result of speed for the Drowsiness detection system using DCT compression will be improved 5% as compared to the one using Haar Wavelet compression. While for the accuracy of the Drowsiness Detection System expected to be 90%.

## Reference:

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